Product Features

- ✧ Four-channel full-duplex active optical cable
- ✧ 25.78Gb/s data rate per channel
- ✧ Available in standard lengths of 3, 5, 7, 10, 15, 20, 30, and 50m
- ✧ Power dissipation < 2.5W per end
- ✧ Built-in digital diagnostic functions
- ✧ Built-in CDR
- ✧ 850nm VCSEL transmitter
- ✧ Good EMI performance
- ✧ Single 3.3V power supply
- ✧ RoHS compliant
- ✧ Operating case temperature: 0~+70°C

Applications

- ✧ 100GBASE-SR4

Ordering Information

Part Number	Output Power	Rec. Sens	Data Rate	Wavelength	Distance
FH-A100M3QQyy			100G		1-50M

General

FH-A100M3QQyy is 100Gb/s QSFP28 active optical cable (AOC).It is compliant with the QSFP28 MSA and IEEE 802.3bm. Crealights QSFP28 AOC is an assembly of four full-duplex lanes, where each lane is capable of transmitting data at rates up to 25.78125Gb/s, providing an aggregated rate of 103.125Gb/s.

ABSOLUTE MAXIMUM RATINGS (TC=25°C, UNLESS OTHERWISE NOTED)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	TS	-40	-	+70	ºC
Maximum Supply Voltage	Vcc	-0.3	-	3.6	V
Operating Relative Humidity	RH	15	-	+85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note.
Data Rate (per lane)	DR	-	25.78125	-	Gb/s	
Bit Rate(per lane)	BR		25.78125		Gb/s	
Bit Error Rate	BER			1×10^{-12}		PRBS31
Operating Case temperature	Tc	0	-	+70	ºC	
Supply Voltage	VCC	3.135	3.3	3.465	V	
Power Consumption(per end)		-	-	2.5	W	
Data Speed Tolerance	ΔDR	-100	-	+100	ppm	

Pin Definitions And Functions

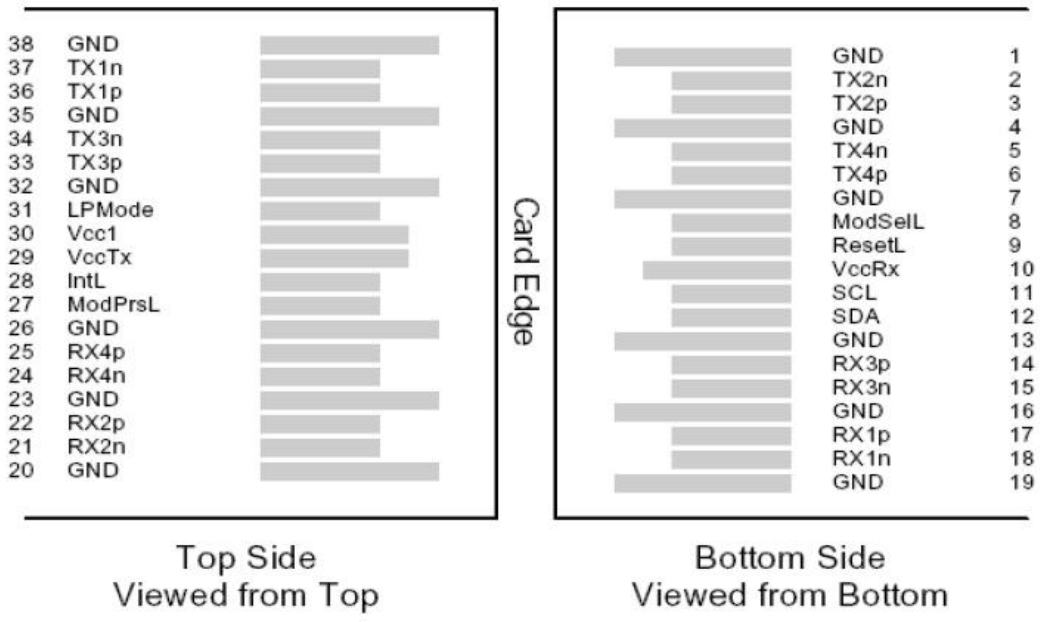


Figure 1 – QSFP28-Compliant 38-Pin Connector (Per SFF-8679)

Pin	Symbol	Name/Description	Ref.
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3 V Power supply receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	2
29	Vcc Tx	+3.3 V Power supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1

Pin	Symbol	Name/Description	Ref.
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

1. Circuit ground is internally isolated from chassis ground.
2. IntL is an open collector/drain output, which should be pulled up with a 4.7k – 10k Ohms resistor on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

DIGITAL DIAGNOSTIC FUNCTIONS

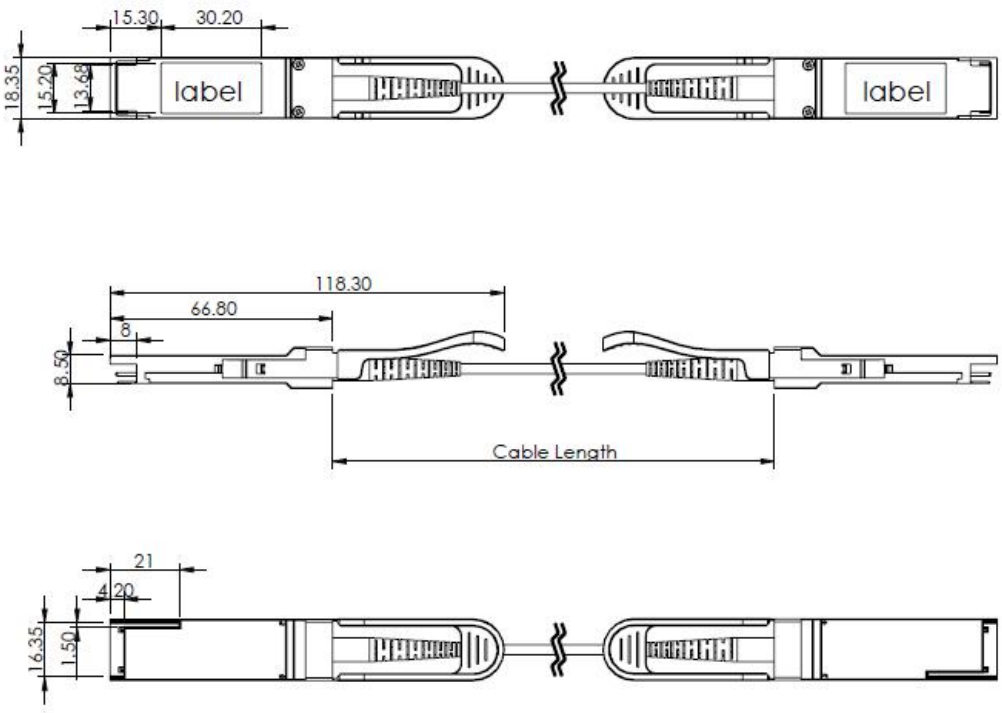
2-Wire Serial Address 1010000x
Lower Page 00h
0 Identifier
1- 2 Status
3- 21 Interrupt Flags
22- 33 Free Side Device Monitors
34- 81 Channel Monitors
82- 85 Reserved
86- 98 Control
99 Reserved
100-104 Hardware Interrupt Pin Masks
105-106 Vendor Specific
107 Reserved
108-110 Free Side Device Properties
111-112 Assigned for use by PCI Express
113 Free Side Device Properties
114-118 Reserved
119-122 Password Change Entry Area (Optional)
123-126 Password Entry Area (Optional)
127 Page Select Byte

Upper Page 00h	Optional Page 01h	Optional Page 02h	Optional Page 03h
128 Identifier	128 CC_APPS	128-255 User EEPROM Data	128-175 Free Side Device Thresholds
129-191 Base ID Fields	129 AST Table Length (TL)		
	130-131 Application Code Entry 0		
	132-133 Application Code Entry 1		
	134-253 other entries		176-223 Channel Thresholds
192-223 Extended ID			224 Tx EQ & Rx Emphasis Magnitude ID
224-255 Vendor Specific ID			225 RX output amplitude indicators
			226-241 Channel Controls
			242-251 Channel Monitor Masks
	254-255 Application Code Entry TL		252-255 Reserved

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through a 2-wire serial interface. The 2-wire serial interface shall consist of a master and slave. The fixed side shall be the master and the free side shall be the slave. Control and data are transferred serially. The master shall initiate all data transfers. Data can be transferred from the master to the slave and from the slave to the master. The 2-wire interface shall consist of clock (SCL) and data (SDA) signals. The master utilizes SCL to clock data and control information on the 2-wire bus.The master and slave shall latch the state of SDA on the positive transitioning edge of SCL.The SDA signal is bi-directional. During data transfer, the SDA signal shall transition when SCL is low. A transition on the SDA signal while SCL is high shall indicate a stop or start condition.
For more information, please see the QSFP28 MSA documentation.

Parameter	Symbol	Accuracy	Units	Notes
Transceiver Case Temperature	DMI_Temp	±3	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	±3%	V	Full operating range
Channel Bias current monitor	DMI_Ibias	±10%	mA	Per channel
Channel RX power monitor absolute error	DMI_RX	±3	dB	Per channel
Channel TX power monitor absolute error	DMI_TX	±3	dB	Per channel

Package Dimensions



For More Information

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